Description

Address generator for generating addresses for testing
a circuit

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The invention relates to an address generator for
generating addresses for testing an addressable
circuit, and in particular for testing an addressable
memory module.

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US 6 031 692 describes a memory system for error
correction with an address generator. The address
generator comprises a base address counter and a
plurality of offset address generators, the base
15 address counter being connected to an input of an
addition circuit. The address generator furthermore
contains a multiplexer circuit which, in a manner
dependent on a selection control signal, through-
connects an offset address generator to a further input
20 of the addition circuit. The addition circuit adds the
address present at the first input to the relative
address value present at the second input.

DE 4 446 988 A1 describes a test pattern generator. The
25 test pattern generator serves for generating addresses
for testing an addressable circuit. In the test pattern
generator, a plurality of arithmetic units are used for
generating the addresses. The test pattern generator
can be operated with a minimal number of control lines
30 by a test device.

After the production operation, circuits are generally
subjected to a test operation in order to test whether
they are functional. Integrated semiconductor circuits,
35 in particular, comprise a multiplicity of components in
order to test their functionality in complicated test
methods.

Figure 1 shows a test arrangement according to the

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prior art. A test device is connected via a data bus
having the bus width D and an address bus having the
bus width A to a circuit to be tested DUT (DUT: Device
under test) and checks the functionality thereof. The
5   circuit to be tested is, for example, a memory having a
multiplicity of memory cells which are arranged in
matrix form and can be addressed via the address bus.
The test device generates, in an address generator, the
addresses of the memory cells to be tested. In a test
10 pattern generator, test data patterns are generated and
applied via the data bus to the memory cells to be
tested. Afterward, the data are read out again from the
memory cells via the data bus and compared with the
expected data in a test evaluation circuit within the
15 test device. The circuit to be tested may be any
desired digital circuit for example a memory, a logic
circuit or a circuit which contains both logic elements
and memory cells. If the data acquired by the test data
evaluation circuit correspond to the expected data
20 values, the test device recognizes that the circuit to
be tested DUT is functional.

Figure 2 diagrammatically shows the construction of a
memory having M×N memory cells SZ which are arranged in
25 matrix form and can be addressed via row addresses X
and column addresses Y. Integrated memories, for
example DRAM memories, are complex circuit arrangements
in which memory cells lying next to one another in the
logical address space are remote from one another in
30 the real circuitry arrangement, for example in a
different layer of the semiconductor memory.
Conversely, memory cells whose logical addresses have a
large difference often adjoin one another. In order to
test interactions between different memory cells, the
35 test program carries out defined jumps from one memory
cell SZ_A to another memory cell SZ_B. The functionality
of the individual memory cells SZ is tested by writing
in data and subsequently reading out data. In order to
test interactions between the memory cells SZ,

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predetermined address patterns are applied to the memory.

The disadvantage of the conventional test arrangement
5 illustrated in figure 1 is that the address bus width A is relatively large, i.e. that many address bus lines have to be led from the test device to the circuit to be tested DUT. If the circuit to be tested DUT is an MxN memory, for example, the number A of address lines
10 is:

$$A = 1dM + 1dN$$

where M is the number of column address lines and N is
15 the number of row address lines of the memory to be tested DUT.

Synchronous DRAM memories already operate at operating frequencies of a few 100 MHz and must be tested by the
20 test device with a corresponding clock frequency. The test arrangement according to the prior art as illustrated in figure 1 has the disadvantage that the number of address lines or the address bus width A is relatively high and the length of the test lines
25 leading from the test device to the circuit arrangement to be tested DUT is large. In order to enable testing of a circuit arrangement operated at high frequency, such as, for example, a DRAM memory, it is necessary, therefore, to use highly complex test devices in the
30 test arrangement illustrated in figure 1, the test frequency of which test devices corresponds to the operating frequency of the circuit arrangement to be tested and which test devices have an address bus width A which is identical to the address bus width of the
35 circuit to be tested (DUT).

The object of the present invention, therefore, is to provide an address generator for generating addresses for testing an addressable circuit which can be

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operated with a minimal number of control lines by a
test device.

This object is achieved according to the invention by
5   means of an address generator having the features
specified in patent claim 1.

The invention provides an address generator for
generating addresses for testing an addressable
10   circuit, having: at least one base address register for
buffer-storing a base address, which base address
register is in each case assigned to an associated
offset register group having a plurality of offset
registers for buffer-storing relative address values; a
15   first multiplexer circuit, which, in a manner dependent
on a base register selection control signal, switches
through an address buffer-stored in the base address
register to a first input of an addition circuit and to
an address bus, which is connected top the circuit to
20   be tested; a second multiplexer circuit, which, in a
manner dependent on the base register selection control
signal, through-connects the offset register group
associated with the through-connected base address
register to a third multiplexer circuit, which, in a
25   manner dependent on an offset register selection
control signal, through-connects an offset register of
the through-connected offset register group to a second
input of the addition circuit; the addition circuit
adding the base address present at the first input to
30   the relative address value present at the second input
to form an address which is written to the base address
register.

In a preferred embodiment of the address generator
35   according to the invention, the base address register
and the associated offset registers can be initialized
by an external test device, via initialization lines.

In a further preferred embodiment of the address

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generator according to the invention, the address
signal switched through to the address bus can be
inverted by a controllable inverting circuit.

5   In a further preferred embodiment of the address
generator according to the invention, the number of
offset registers of an offset register group is equal
to the number of address test jump variants required
for testing the circuit.
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In a further preferred embodiment of the address
generator according to the invention, the circuit to be
tested is a synchronous memory which is operated with a
high operating clock frequency.
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The memory preferably has a multiplicity of memory
cells which can be addressed via a multidimensional
address space.

20   In this case, the number of base address registers
preferably corresponds to the dimension of the address
space of the memory to be tested.
In a particularly preferred embodiment of the address
generator according to the invention, the base address
25   register selection control signals and the offset
register selection control signals are applied to the
address generator by an external test device via an
address control signal bus, the bus width of the
address control signal bus between the test device and
30   the address generator being less than the bus width of
the address bus between the address generator and the
circuit to be tested.

The length of the address bus lines between the address
35   generator and the circuit to be tested is preferably
much smaller than the length of the address control
lines between the test device and the address
generator.

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In a particularly preferred embodiment, the address generator is integrated in the circuit to be tested.

5 Preferred embodiments of the address generator according to the invention are described below with reference to the accompanying figures for elucidating features that are essential to the invention.

In the figures:
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figure 1 shows a test arrangement according to the prior art;

figure 2 shows a memory to be tested, having a
15 plurality of memory cells;

figure 3 shows a test arrangement in which the address generator according to the invention is used;

20 figure 4 shows a particularly preferred embodiment of the address generator according to the invention.

Figure 3 illustrates a test arrangement in which the address generator 1 according to the invention is used.
25 The address generator 1 serves for generating addresses for testing an addressable circuit 2 to be tested. The address generator 1 and the circuit 2 to be tested are connected to one another via an address bus 3. The address generator 1 applies via the address bus 3
30 successive addresses of memory cells or addressable components to be tested within the circuit 2. In the test arrangement illustrated in figure 3, the address generator 1 is situated in a test circuit 4 designed, for example, as an application-specific integrated
35 circuit (ASIC). In addition to the address generator 1, the test circuit 4 contains a circuit 5 for generating test data patterns and evaluating them. The circuit 5 is likewise connected to the circuit 2 to be tested, via a data bus 6 having the data bus width D. The data

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pattern generator 5 generates test data patterns which
are written to the addressed memory cells via the data
bus 6 and are subsequently read out again via the data
bus 6. The data read out are compared with the expected

5   data through test data of the evaluation circuit 5. The
test data pattern generator and evaluation circuit 5 is
driven by an external conventional test device 8 via a
data control line bus 7 having the bus width Z_D. The
test device 8 drives the address generator 1 according

10   to the invention within the test circuit 4 via an
address control line bus 9. Furthermore, the test
device 8 is connected to the address generator 1 via
initialization lines 10 and via an inversion control
line 11.

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In a first embodiment, in an application-specific
integrated circuit ASIC, the test circuit 4 is provided
as an autonomous semiconductor circuit between the
actual test device 8 and the circuit arrangement 2 to

20   be tested. In an alternative embodiment, the test
arrangement 4 is integrated into the circuit
arrangement 2 to be tested. In both embodiments, the
length of the address bus lines of the address bus 3
between the address generator 1 and the circuit

25   arrangement 2 to be tested is significantly smaller
than the length of the address control lines between
the test device 8 and the address generator 1. As a
result of this, the address test signals present on the
address bus 3 are significantly more robust relative to

30   high-frequency interference signals which originate
e.g. from other address lines. Furthermore, the address
test signals are degraded to a much lesser extent by
the address lines, so that the signal edges of the
address signals which arrive at the circuit 2 to be

35   tested are relatively steep, thereby avoiding errors
during the testing of the circuit arrangement 2.

Figure 4 shows a particularly preferred embodiment of
the address generator 1 according to the invention. The

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address generator 1 contains a plurality of base
address registers 12a, 12b, ... The base address
registers 12 serve for buffer-storing a base address
which can be initialized by the external test device 8
5   via the initialization lines 10. Each of the base
address registers 12 is assigned an offset register
group 13. With the embodiment illustrated in figure 4,
the offset register group 13a, which has a plurality of
offset registers 13a-1, 13a-2, 13a-3, 13a-4 for buffer-
10   storing relative address values, is assigned to the
base address register 12a for the X address or row
address of the memory 2 to be tested. A second offset
register group 13b, which comprises a plurality of
offset registers 13b-1, 13b-2, 13b-3, 13b-4, is
15   assigned to the second base address register 12b for
buffer-storing the Y address or column address of the
memory 2. The relative address values of the different
offset registers of an offset register group 13a, 13b
can likewise be set or programmed by the test device 8
20   via initialization lines 10.

The number of offset registers within an offset
register group 13a, 13b is four in the exemplary
embodiment illustrated in figure 4 and corresponds to
25   the number of required jump variants for testing the
circuit arrangement 2. A wide variety of test jump
variants can be programmed into the address generator 1
according to the invention by the test device 8 via the
initialization lines 10. If, in one test jump variant,
30   for example, the same memory cell is to be tested
again, the relative address values which are written to
the corresponding offset registers 13a-i, 13b-i of the
offset register groups 13a, 13b are zero in each case.
If, in a further test jump variant, the memory cell of
35   the next column within the memory 2 is to be tested,
the relative address value is zero in the offset
register 13a-i and one in the offset register 13b-i.
If, in a further test jump variant, for example, the
memory cell of the next but one column and next row is

to be tested, the relative address value of the offset
register 13a-i is one and the relative address value of
the offset register 13b-i is two.

5   In the exemplary embodiment illustrated in figure 4, it
is possible to program four different test jump
variants. In further embodiments (not illustrated) of
the address generator 1 according to the invention,
correspondingly more offset registers are provided for
10   increasing the possible test jump variants.

The offset registers of the offset register groups 13a,
13b are connected via lines 14a, 14b to inputs 15a, 15b
of multiplexers 16 within a first controllable
15   multiplexer circuit 17. The multiplexers 16-1 to 16-4
within the first multiplexer circuit 17 each have
control inputs 18, which are connected via lines 19 to
a control input 20 of the first multiplexer circuit 17.
Furthermore, the multiplexers 16-1 to 16-4 within the
20   first multiplexer circuit 17 have outputs 21, which are
connected via lines 22 to inputs 23 of multiplexers 24
within a multiplexer circuit 25. The multiplexers 24-1
to 24-2 within the multiplexer circuit 25 have control
inputs 26, which are connected via control lines 27 to
25   a control input 28 of the multiplexer circuit 25.
Furthermore, the multiplexers 24-1, 24-2 have outputs
29, which are connected via lines 30 to inputs 31 of a
further multiplexer 32 connected downstream in a
cascade-type manner within the multiplexer circuit 25.
30   The multiplexer 32 connected downstream has a control
input 33, which is connected via a control line 34 to a
further control input 28-2 of the multiplexers 25. The
multiplexer 32 has an output 35, which is connected via
a line 36 to an output 37 of the multiplexer circuit
35   25.

In addition to the multiplexer circuit 17 and the
multiplexer circuit 25, the address generator 1
according to the invention, as is illustrated in figure

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4, contains a further multiplexer circuit 38, which, in
a manner dependent on the base register selection
control signal present on the control line 9 switches
through an address buffer-stored in the base address

5 registers 12-1, 12-2 from a first input of an addition
circuit to an address bus of the circuit 2 to be
tested. For this purpose, the multiplexer circuit 38
has a control input 39, which is connected to the
control line 9. The multiplexer circuit 38 has a first

10 input 40, which is connected via a line 41 to the first
base address register 12a for buffer-storing the row
address X, and a second input 42, which is connected
via a line 43 to the second base address register 12b
for buffer-storing the column address Y. The control

15 inputs 39 of the multiplexer circuit 38 and the control
input 20 of the multiplexer circuit 17 receive the same
base register selection control signal via the control
line 9. For this purpose, the control input 20 of the
multiplexer circuit 17 is likewise connected to the

20 control line 9 to form a control line 44. If, in a
manner dependent on the base register selection control
signal applied on the control line 9, a base address
register 12-i is through-connected by the first
multiplexer circuit 38 to the output 45 thereof, all

25 the offset registers of the offset register group 13
associated with the through-connected base register 12
are simultaneously through-connected by the multiplexer
circuit 17 to the multiplexer circuit 25.

30 The control inputs 28-1, 28-2 of the multiplexer
circuit 25 are connected to a control terminal 47 of
the address generator 1 via lines 46. The control input
20 of the multiplexer circuit 17 is connected via a
line 44 and the control input 39 of the multiplexer

35 circuit 38 is connected via a line 48 to a further
control terminal 49 of the address generator 1
according to the invention. The control inputs 47, 49
are driven by the external test device 8 via address
control lines of the address control line bus 9.

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Furthermore, the test device 8 is connected via
initialization lines 10 to an initialization terminal
50 of the address generator 1. The initialization
terminal 50 is connected to the base address registers
5   12a, 12b via internal initialization lines 51 and to
the offset registers 13 via internal initialization
lines 52.

In the embodiment illustrated in figure 4, the output
10   55 of the multiplexer circuit 38 is connected via lines
53 to an inverting circuit 54. The inverting circuit 54
is e.g. an XOR logic circuit connected via internal
lines 55 to a control terminal 56 of the address
generator 1 according to the invention. The control
15   terminal 56 receives an inversion control signal from
the external test device 8 through lines 11. The
inversion circuit 54 makes it possible, as required, to
invert address signals for testing the circuit
arrangement 2 bit by bit.
20

At the branching node 57 the address switched-through
by the multiplexer circuit 45 is applied via lines 58
to a first input 59 of an addition circuit 60. The
addition circuit 60 has a second input 61, which is
25   connected via lines 62 to the output 37 of the
multiplexer circuit 25. The addition circuit 60 adds
the switched-through base address present at the first
input 59 to the relative address value which is present
at the second input 61 and is switched through by the
30   multiplexer circuit 25 in a manner dependent on the
offset register selection control signal, to form a
summation address value which is written via an output
63 and lines 64 to the base address register 12 for
generating the next address. The controllable inversion
35   circuit 54 has an output 65, which is connected via
internal lines 66 to an output 67 of the address
generator 1 according to the invention.

In order to test the circuit arrangement 2, firstly the

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base addresses are initialized by the test device 8 via
the initialization lines 10 and written to the base
address registers 12. Furthermore, the relative jump
values of the different test jump variants to be tested
5   are initialized by the writing of relative address
values to the offset registers 13. A base address is
selected by the application of a base register
selection control signal to the control terminal 49 via
address control lines 9. Afterward, the desired test
10 jump variant or the desired relative address value is
selected by the application of an offset register
selection control signal to the control input 47 of the
address generator 1. The addressed memory cell is
subsequently tested by applying and reading out data.
15 The operation is repeated until it is identified that
the test operation has ended.

In the exemplary embodiment illustrated in figure 4,
the number Z_A of required control lines 9 of the
20 address control signal bus 9 for controlling the
address jumps is three.

Generally the number Z_A of required control lines for
the driving of the address generator 1 by the external
25 test device 8 is:

$$Z_A = 1dd + 1dp$$

where d is the dimension of the address space of the
30 circuit arrangement 2 to be tested, and
p is the number of desired test jump variants.

In the example illustrated in Figure 4, a memory Z
arranged in a matrix-type manner with a two-dimensional
35 address space d=2 is tested, the number of possible
test jump variants p being four in the example
illustrated. The number of required control lines for
the driving of the address generator is thus three.

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In a memory 2 having 1024 ($=2^{10}$) column addresses and
1024 ($=2^{10}$) row addresses, the address bus width A of
the address bus between the address generator 1 and the
memory is at least ten, while the number Z_A of required
5   control lines for the driving of the address generator
1 by the external test device 8 comprises merely three
lines. Consequently, the number Z_A of required address
control lines for the driving of the address generator
1 by the test device 8 is significantly less than the
10   width of the address bus 3. If the test arrangement 4
comprising the address generator 1 is positioned, as
application-specific integrated circuit (ASIC), in
spatial proximity to the circuit arrangement 2 or if
the test arrangement 4 is even integrated into the
15   circuit arrangement 2, the length of the address
control lines of the address control line bus 9 is
significantly greater than the length of the address
lines between the address generator 1 according to the
invention and the circuit arrangement 2 to be tested.
20   The control signals on the address control lines which
are output from the test device 8 to the address
generator 1 according to the invention have a
significantly lower clock frequency than the clock
frequency with which the generated addresses are
25   applied from the address generator 1 to the circuit
arrangement 2 for testing.

In the test arrangement according to the invention as
illustrated in figure 3, it is therefore possible to
30   use an external test device 8 with a relatively low
operating frequency, the test device 8, moreover, only
having to have a very small number of address control
lines. In the test arrangement according to the
invention as illustrated in figure 3, it is therefore
35   possible to use conventional test devices 8 which
operate with a relatively low operating frequency, for
testing memory modules 2 which operate with a
considerably higher clock frequency of a few 100 MHz,
without necessitating a considerable additional outlay

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on circuitry.

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List of reference symbols

1.   Address generator
2.   Circuit to be tested
3.   Address bus
4.   Test circuit
5.   Test pattern generator and evaluation circuit
6.   Data bus
7.   Data control line bus
8.   Test device
9.   Address control line bus
10. Initialization lines
11. Inversion control line
12. Base address register
13. Offset register
14. Line
15. Multiplexer input
16. Multiplexer
17. Multiplexer circuit
18. Control inputs
19. Control line
20. Control input
21. Output
22. Lines
23. Multiplexer input
24. Multiplexer
25. Multiplexer circuit
26. Control input
27. Control line
28. Control input
29. Output
30. Line
31. Input
32. Multiplexer
33. Control input
34. Control line
35. Output
36. Line
37. Output

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38. Multiplexer circuit
39. Control input
40. Input
41. Line
42. Input
43. Line
44. Control line
45. Output
46. Control lines
47. Control input
48. Control line
49. Control input
50. Initialization terminal
51. Initialization lines
52. Initialization lines
53. Line
54. Inversion circuit
55. Control line
56. Control input
57. Branching node
58. Line
59. Input
60. Addition circuit
61. Input
62. Line
63. Output
64. Lines
65. Output
66. Line
67. Address output